UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/631,824	08/01/2003	Xavier Montagne	003921.00143	1708

22907 7590 04/01/2009

BANNER & WITCOFF, LTD.
1100 13th STREET, N.W.
SUITE 1200
WASHINGTON, DC 20005-4051

EXAMINER	
TABLER, MATTHEW C	
ART UNIT	PAPER NUMBER
2819	

MAIL DATE	DELIVERY MODE
04/01/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/631,824	MONTAGNE ET AL.	
	Examiner	Art Unit	
	MATTHEW C. TABLER	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 March 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15,35 and 36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15,35 and 36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This office action is in response to applicant's remarks filed on March 16th, 2009. Currently, claims 1-15 and 35-36 are pending.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-15 and 35-36 are rejected under 35 U.S.C. 102(b) as being anticipated by New et al. (US Patent 6,292,019) patented on September 18th, 2001.

Regarding claim 1, New et al. show an integrated circuit (Figure 3), comprising a reconfigurable interconnect portion (MUX 320A), a data processing portion (control circuit 330) coupled to the reconfigurable interconnect portion (320A), the data processing portion (330) configured to provide a bit pattern to the reconfigurable interconnect portion to load a configuration of the reconfigurable interconnect portion (control circuit 330 configures 320A), and a storage unit (LUT's 335 and 337) coupled to the data processing portion (330), the storage unit including a configuration bit look-up table (LUT's 335 and 337), wherein the data processing portion (330) is configured to extract a set of bits from the configuration bit look-up table (335, 337) to map a common plurality of inputs of the reconfigurable interconnect portion (selected inputs of 320A) to a plurality of outputs of the reconfigurable interconnect portion (320A output).

Regarding claim 2, New et al. show the integrated circuit includes a second reconfigurable interconnect portion (320B, not shown in figure), and the configuration bit look-up table (335, 337) is configured to allow the data processing portion to extract a first set of configuration bits representing the bit pattern (controls 320A) and to extract a second set of configuration bits representing a second bit pattern to load a second configuration of the second reconfigurable interconnect portion (controls 320B), wherein the second set is a subset of the first set (first and second sets are subsets of control signals C1-C4).

Regarding claim 3, New et al. show the reconfigurable interconnect portion comprises a switching matrix (320A).

Regarding claim 4, New et al. show reconfigurable interconnect portion comprises a multiplexer (320A).

Regarding claim 5, New et al. show the switching matrix includes a control signal input configured to select between two inputs to connect to an output (control signals select output from inputs).

Regarding claim 6, New et al. show the reconfigurable interconnect portion comprises a pair of transistors (conventional design of a 2:1 MUX includes two transistors receiving two inputs wherein the control signal turns one transistor ON (passes input signal) and turns one OFF (blocking input signal).

Regarding claim 7, New et al. show the reconfigurable interconnect portion comprises a plurality of memory elements (multiplexer's are LUT memories), each memory element connected to at least one switch of the reconfigurable interconnect

portion (each input line of the multiplexer has a switch or transistor that is programmed by the control signal).

Regarding claim 8, New et al. show the bit pattern is derived from the configuration bit look-up table (335, 337).

Regarding claim 9, New et al. show the configuration bit look-up table comprises a plurality of rows of configuration bits (335 and 337 each have a row).

Regarding claim 10, New et al. show the storage unit (335, 337) is coupled to the data processing portion (330) by a plurality of address lines for accessing the rows of configuration bits stored within the storage unit (address lines shown in blown up view of 330 in bottom, left of Figure 3).

Regarding claim 11, New et al. show the storage unit further comprises programming instructions (C1-C4) configured for accessing the configuration bit look-up table (control signals access 335, 337), wherein the programming instructions are further configured for extracting a subset of configuration bits from the configuration bit look-up table (C1-C4 configure LUT's 335, 337 which configure processor 330 and configure interconnect 320A).

Regarding claim 12, New et al. show the data processing portion (330) is configured to map a first input of the common plurality of inputs of the reconfigurable interconnect portion (selects first input of 320A) to a first output of the plurality of outputs of the reconfigurable interconnect portion in response to a first command (output of 320A; selected by control signals).

Regarding claim 13, New et al. show the data processing portion (330) is configured to map a second input of the common plurality of inputs of the reconfigurable interconnect portion (selects second input of 320A) to a second output of the plurality of outputs of the reconfigurable interconnect portion in response to the first command (output of 320A; selected by control signals).

Regarding claim 14, New et al. show the data processing portion (330) is configured to map a second input of the common plurality of inputs of the reconfigurable interconnect portion (second input of 320A) to a second output of the plurality of outputs of the reconfigurable interconnect portion in response to a second command (output of 320A; selected by control signals).

Regarding claim 15, New et al. show a second reconfigurable interconnect portion (320B), and wherein the data processing portion (330) is configured to map a first input of the second reconfigurable interconnect portion (first input of 320B) to a first output of the second reconfigurable interconnect portion in response to a second command (output of 320B; selected by control signals).

Regarding claim 35, New et al. show an integrated circuit comprising a reconfigurable interconnect portion (320A) and a storage unit (335, 337) coupled to the reconfigurable interconnect portion, wherein the storage unit stores a look-up table for use in configuring the reconfigurable interconnect portion (LUT's 335, 337), wherein a data processing portion (330) is configured to extract from the look-up table a set of bits to map a common plurality of inputs of the reconfigurable interconnect portion to a

plurality of outputs of the reconfigurable interconnect portion (controls signals map inputs to outputs of 320A).

Regarding claim 36, it has been rejected on the same grounds as claim 2.

Response to Arguments

Applicant's arguments with respect to claims 1-15 and 35-36 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MATTHEW C. TABLER whose telephone number is (571)270-1567. The examiner can normally be reached on Monday through Friday 8:30AM-6:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rexford Barnie can be reached on (571) 277-3749. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/M. C. T./
Examiner, Art Unit 2819
March 31, 2009

/Vibol Tan/
Primary Examiner, Art Unit 2819